[English Translation of Excerpt from Reference 2]

Laid-Open Japanese Patent Application 2003-234325 A
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Inventors: Riichiro MIHASHI, Masabumi KUBOTA and Shigenori HAYASHI [all of JP]
Title of Invention: MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICES
--- (omitted) ---
[Claims]
[Claim 1] A wet etching method comprising:
a first step of thermally treating a metal oxide film-deposited substrate;
a second step of exposing the thermally treated surface of said metal oxide film to plasma; and
a third step of removing at least said plasma-exposed surface portion of said metal oxide film by wet etching.
[Claim 2] The wet etching method according to Claim 1, wherein said second step comprises a step of applying bias power on said substrate.
[Claim 3] The wet etching method according to Claim 1, wherein said plasma is a plasma comprising HBr-containig gas.
[Claim 4] The wet etching method according to Claim 1, wherein said third step is executed by using a fluorine-containing solution.
[Claim 5] The wet etching method according to Claim 1, wherein said metal oxide film is an oxide film containing at least one of hafnium, zirconium, lanthanum, tantalum and aluminum.
[Claim 6] A manufacturing method for semiconductor devices comprising:
a first step of thermally treating a metal oxide film-deposited substrate;
a second step of depositing a conductive film on said thermally treated metal oxide film;
a third step of forming a gate electrode by patterning said conductive film and exposing the external side portion of said gate electrode in said metal

oxide film;
a fourth step of exposing the surface of said metal oxide film in its exposed portion to plasma; and
a fifth step of removing said plasma-exposed metal oxide film in its exposed portion by wet etching.
[Claim 7] The manufacturing method for semiconductor devices according to Claim 6, wherein said third step comprising a step of successively plasma-etching said conductive film and metal oxide film using a mask pattern covering the gate electrode formation area and thereby thinning the external side portion of said gate electrode in said metal oxide film.
[Claim 8] A manufacturing method for semiconductor devices comprising:
a first step of forming a dummy gate electrode on a substrate;
a second step of forming an insulating side wall on the side surface of said dummy gate electrode;
a third step of forming an interlayer insulation film on said dummy gate- and side wall-formed substrate so that the upper surface of said dummy gate electrode can be exposed;
a fourth step of removing said dummy electrode and thereby forming, on said interlayer insulation film, a recess which has said side wall as a wall surface;
a fifth step of depositing a metal oxide film on said interlayer insulation film so that said recess can be part way filled;
a sixth step of thermally treating said metal oxide film-deposited substrate;
a seventh step of depositing a conductive film on said thermally treated metal oxide film so that said recess can be completely filled;
an eighth step of removing the external side portion of said recess in said conductive film so that a gate electrode can be formed in said recess and the external side portion of said recess in said metal oxide film can be exposed;
a ninth step of exposing the surface of said metal oxide film in its exposed portion to plasma; and
a tenth step of removing the plasma-exposed portion of said metal oxide film in its exposed portion by wet etching.
[Claim 9] The manufacturing method for semiconductor devices according to Claim 8, wherein said first step comprises a step of forming a dummy insulation film between said substrate and said dummy gate electrode, and said fourth step comprises a step of removing said dummy gate insulation film.

[Claim 10] The manufacturing method for semiconductor devices according to Claim 8, wherein said ninth step comprises plasma-etching the exposed portion of said metal oxide film and thereby thinning the exposed portion of said metal oxide film.

--- (omitted) ---

[0033]

[Embodiments of Invention] (First Embodiment) In the following, a wet etching method according to a first embodiment of the present invention shall be explained in reference to Figures.

[0034] Figures 3 (a)~(d) are cross sectional views for respective steps of a wet etching method according to the first embodiment.

[0035] First, for example, using a sputtering vapor deposition device, an HfO_2 film (HfO_2 film immediately after deposition) (12) is deposited on a silicon substrate (11).

[0036] Then, the silicon substrate (11) is thermally treated, for example, by treating for rapid thermal nitriding (RTN treatment). Thereby, the HfO_2 film (12) immediately after deposition is altered to an HfO_2 film (HfO_2 film after thermal treatment) (12a), which cannot be wet-etched. Herein, specific thermal treatment conditions include the chamber atmosphere of nitrogen, the thermal treatment temperature of 800°C, and the thermal treatment period of 60 seconds.

[0037] Next, for example, using a inductively coupled plasma (ICP)-type dry etching device, the HfO_2 film after thermal treatment (12a) is exposed to plasma to provide plasma damage to the surface of the HfO_2 film after thermal treatment (12a). Specific plasma gas treatment conditions include the plasma gas comprising a mixture of HBr gas, Cl_2 gas and O_2 gas (in the flow rate ratio of $HBr:Cl_2:O_2=100:15:10$); the total pressure within the chamber of the dry etching device at 8Pa; the bias power applied on the silicon substrate of 60W; and the source power for plasma generation of 500W. By running such a plasma treatment, a wet-etchable damage layer (12b) in an approximate depth of 1~3nm from the surface can be formed by ions (13) in plasma, etc. in a region of the thermally treated HfO_2 film (12a) as shown in Figure 3(c).

[0038] Next, as shown in Figure 3(d), the damage layer(12b) is wet etched, for example, using a dilute hydrofluoric acid (DHF) containing about 1% by mass of hydrofluoric acid, and thereby the damage layer (12b), namely the

surface portion of the thermally treated HfO_2 film (12a) is removed by wet etching.

[0039] According to the first embodiment of the present invention, after the HfO_2 film (12)-deposited silicon substrate (11) has been thermally treated, the surface of the thermally treated HfO_2 film (12a) is exposed to plasma, and subsequently the surface portion of the thermally treated HfO_2 film (12a) is removed by wet etching. Namely, the surface of the HfO_2 film (12a), which has become poorly wet-etchable upon the modification with thermal treatment, is exposed to plasma. Thereby, a damage layer (12b) which can be easily etched is formed on the surface portion of the heat treated HfO_2 film (12a). Accordingly, the damage layer (12b), namely the surface portion of the heat treated HfO_2 film (12a) can be reliable removed by wet etching.

[0040] Also according to the first embodiment, bias power is applied on the silicon substrate in the plasma exposure of the surface of the thermally treated HfO_2 film (12a). This results in the more efficient delivery of ions within plasma to the silicon substrate (11) so that larger plasma damage can be provided to the HfO_2 film (12a), and therefore, the wet etching of the HfO_2 film (12a) can be more simply executed.

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[Brief Explanation of Figures]

[Figure 1] A chart summarizing research results about the changed thicknesses of HfO_2 film by immersing the thermally treated HfO_2 film, which the present inventors obtained, in various kinds of chemical solutions.

[Figure 2] A chart summarizing research results about the dependency of the wet-etched amounts of the thermally treated HfO_2 film, which the present inventors obtained, on the time periods of plasma processing.

[Figure 3] Cross sectional views (a)~(d) respectively showing the steps of a wet etching method according to the first embodiment of the present invention.

[Figure 4] Cross sectional views (a)~(c) respectively showing the steps of a manufacturing method for semiconductor devices according to the second embodiment of the present invention.

[Figure 5] Cross sectional views (a)~(c) respectively showing the steps of a manufacturing method for semiconductor devices according to the second embodiment of the present invention.

[Figure 6] A chart summarizing comparative results of respective dry etching

rates for the thermally treated and thermally non-treated HfO_2 films, which the present inventors obtained.

[Figure 7] Cross sectional views (a)~(d) respectively showing the steps of a manufacturing method for semiconductor devices according to the third embodiment of the present invention.

[Figure 8] Cross sectional views (a)~(c) respectively showing the steps of a manufacturing method for semiconductor devices according to the third embodiment of the present invention.

[Code Explanation]

(11) Silicon substrate; (12) HfO_2 film immediately after deposition; (12a) HfO_2 film after thermal treatment; (12b) Damage layer; (13) Ions in plasma; (21) Silicon substrate; (22) Element isolating insulation film; (23) HfO_2 film immediately after deposition; (23a) HfO_2 film after thermal treatment; (23b) Damage layer; (24) Polysilicon film; (24a) Gate electrode; (25) Mask pattern; (51) Silicon substrate; (52) Element isolating insulation film; (53) Dummy gate insulation film; (54) Dummy gate electrode; (55) Gate side wall insulation film; (56) Interlayer insulation film; (57) Recess; (58) HfO_2 film immediately after deposition; (58a) HfO_2 film after thermal treatment; (58b) Damage layer; (59) Tungsten film; (59a) Gate electrode; and (60) Ions in plasma.

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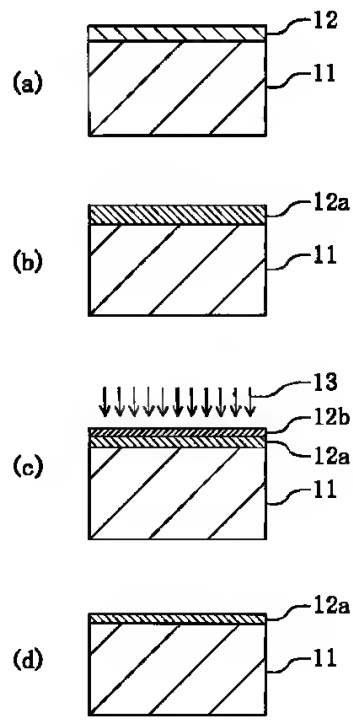
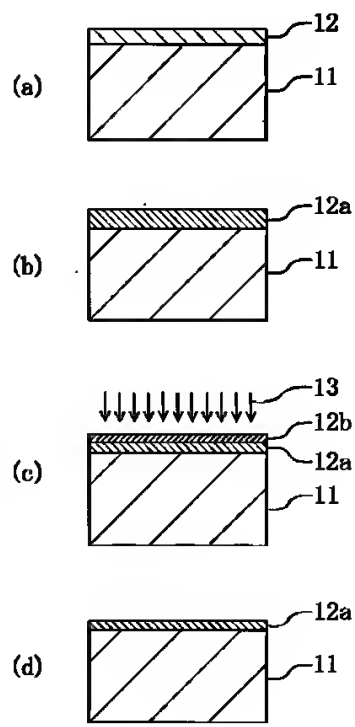
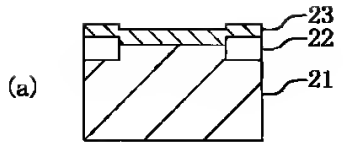
(54)【発明の名称】　半導体装置の製造方法



薬液	濃度(%)	時間(min)	Δ(Å)	備考
KOH	2(重量%)	3	-2	
HCL	3.5	3	6	
HF	50	1	4	
HF	10	3	0	はがれ
ﾌｯｲ化ｱﾝﾓ	4	3	0	
HF	1.2	3	-4	
HF	1.2	3	0	
HF	10	0.5	3	
HF	10	1	10	
HF	5	1	-4	
HF	5	2	231	はがれ
HF+NH4OH	1	1	-1	(原液:HF 1%50ml+NH3 10%1ml)
HF+NH4OH	1	1	0	(原液:HF 1%50ml+NH3 10%2ml)
HF+NH4OH	1	1	0	(原液:HF 1%50ml+NH3 10%3ml)
HF+NH4OH	1	1	-5	(原液:HF 1%50ml+NH3 10%10ml)
硫酸	10	1	1	
硫酸	10	3	0	
塩酸	10	1	-3	
塩酸	10	3	-4	
硝酸	10	3	4	
硝酸	10	1	-5	
ﾘﾝ酸	10	1	1	
ﾘﾝ酸	10	3	-1	
過水	10	3	1	
過水+HF	10+10	1.6	0	はがれ
過水+HF	3+1	1	6	(H2O2 3%50ml+HF 1%50ml)
過水+HF	3+1	3	10	(H2O2 3%50ml+HF 1%50ml)
酢酸	原液	1	4	
酢酸	原液	3	1	
ﾋﾄﾞﾗｼﾞﾝ	40	1	-2	
ﾋﾄﾞﾗｼﾞﾝ	40	3	1	
P.S.ｴｯﾁ液	原液	1	-15	(硝酸:酢酸:ﾌｯ酸=200:80:3)
P.S.ｴｯﾁ液	原液	3	-117	はがれ(硝酸.酢酸.ﾌｯ酸=200.80:3)
ｱﾝﾓﾆｱ	30	1	7	
ｱﾝﾓﾆｱ	30	3	4	
HF+過水	2+3	3	-2	
HF+過水	2+3	6	1	

	ﾌﾟﾗｽﾞﾏｶﾞｽ種	
	HBr+Cl2+O2	HBr+Cl2
ﾌﾟﾗｽﾞﾏ処理時間[min]	ｳｪｯﾄｴｯﾁ量[Å]	ｳｪｯﾄｴｯﾁ量[Å]
1.0		9.5
2.0	17.5	21.7
4.0	13.8	18.3
5以上		28.1

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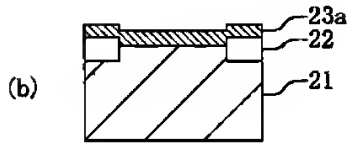
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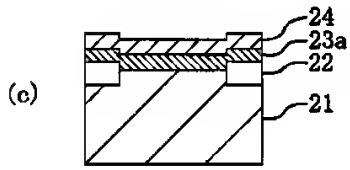
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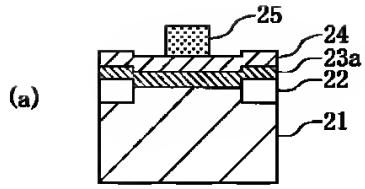
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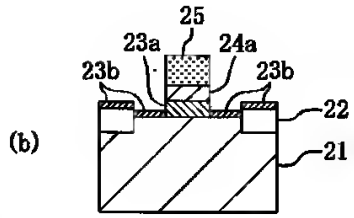
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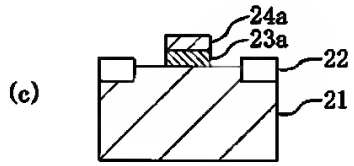
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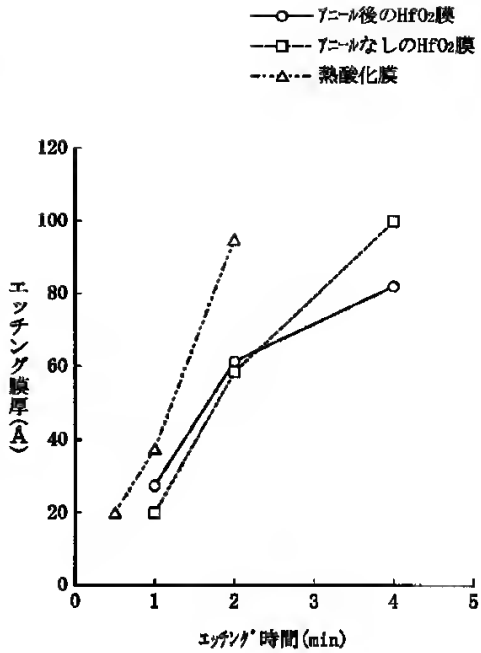
アニール後のHfO2膜
アニールなしのHfO2膜
熱酸化膜
エッチング膜厚(Å)
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60
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20
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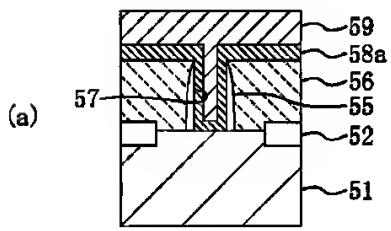
1
2
3
4
5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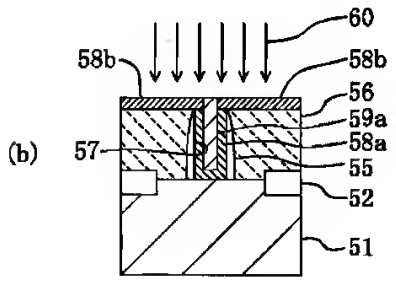
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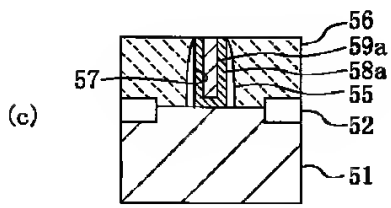
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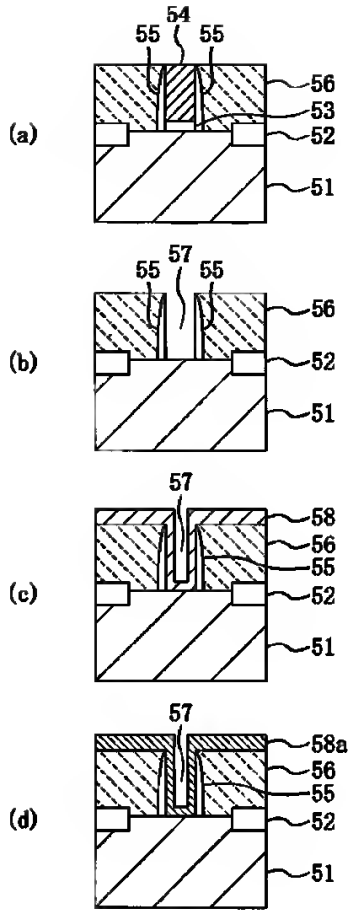
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(d)
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